

FIG. 1

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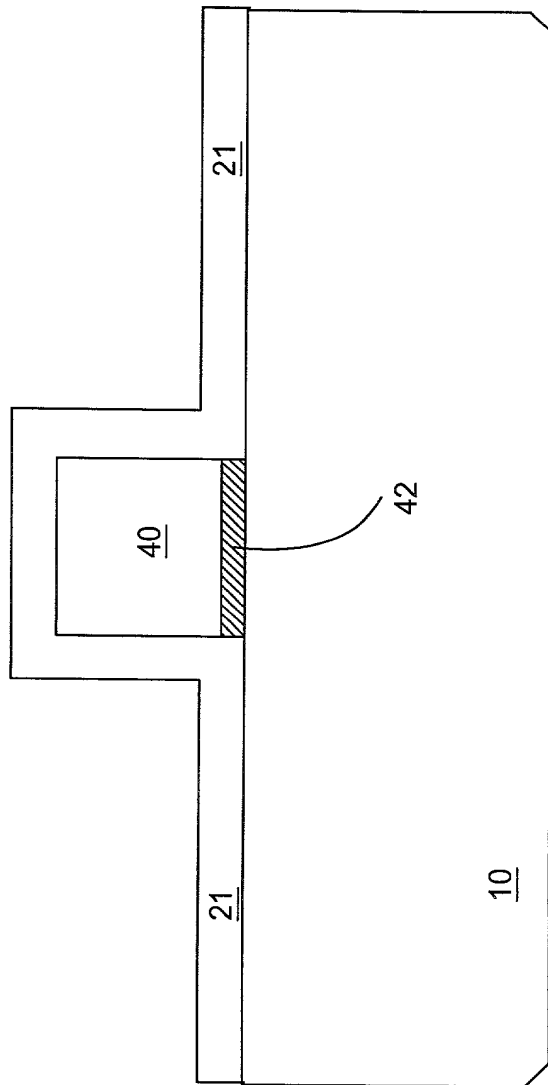


FIG. 2

11

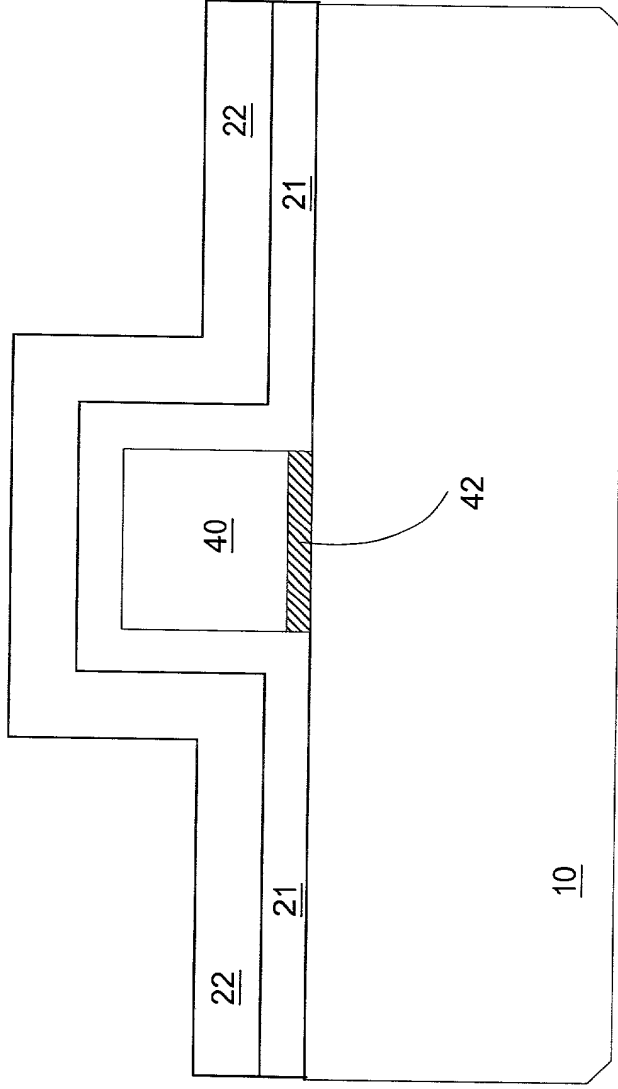


FIG. 3

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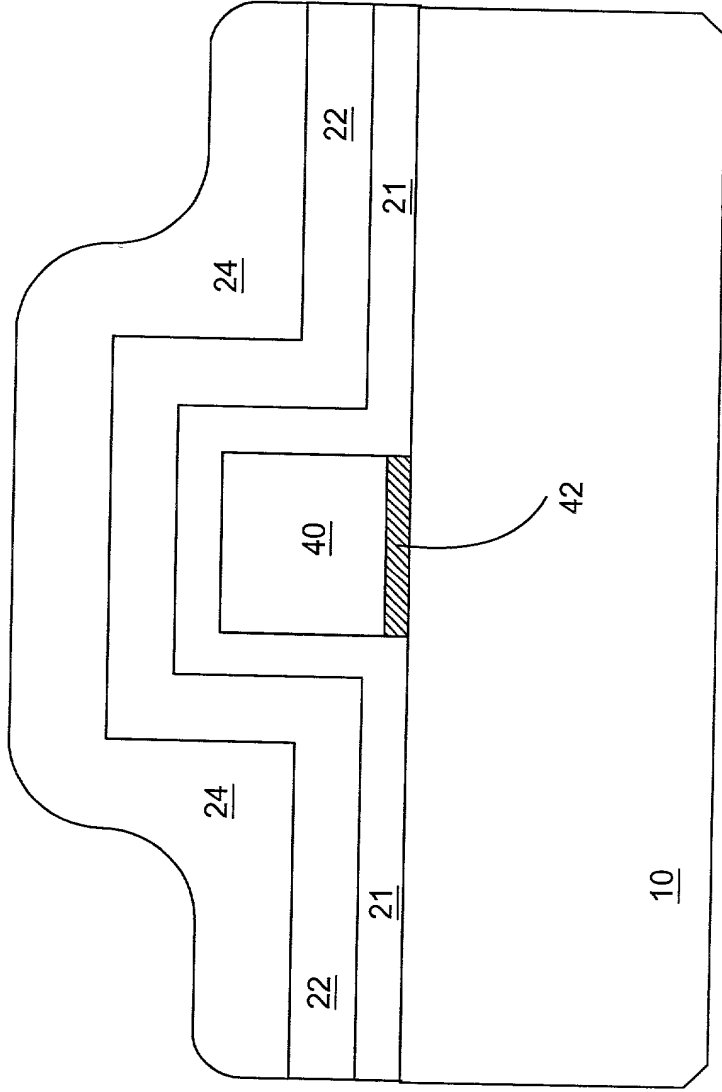


FIG. 4

11

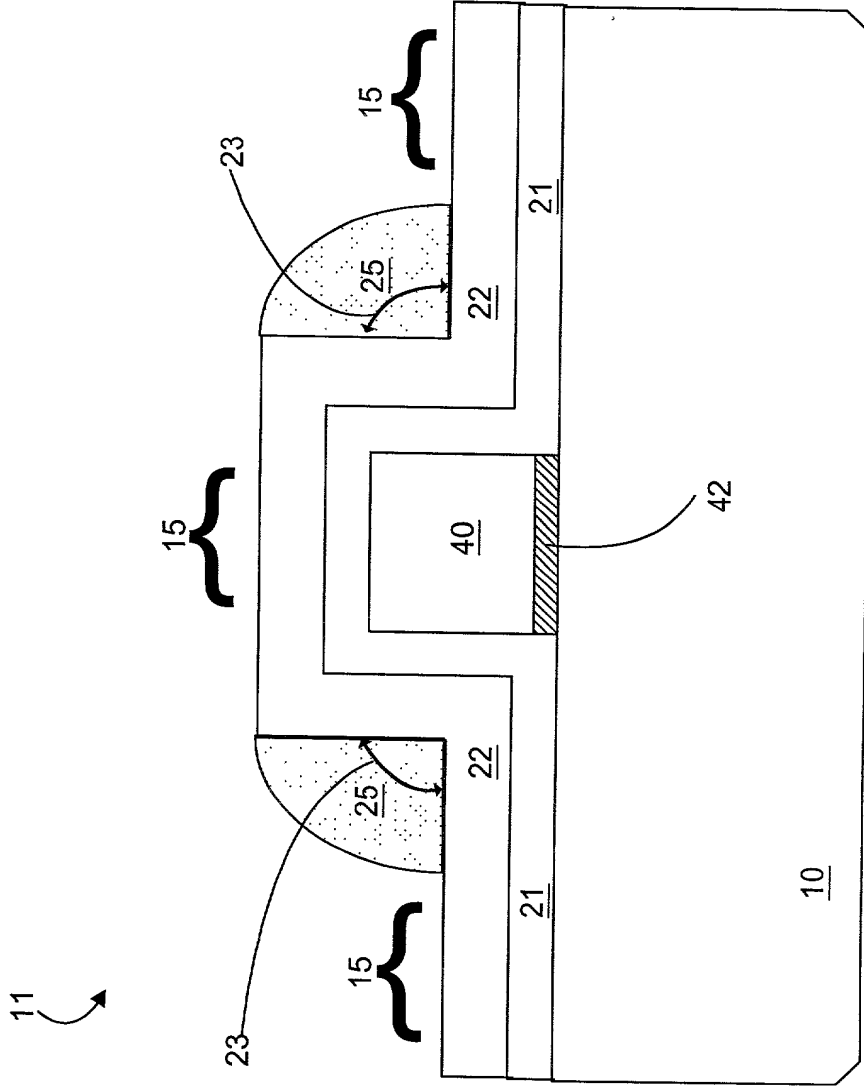


FIG. 5

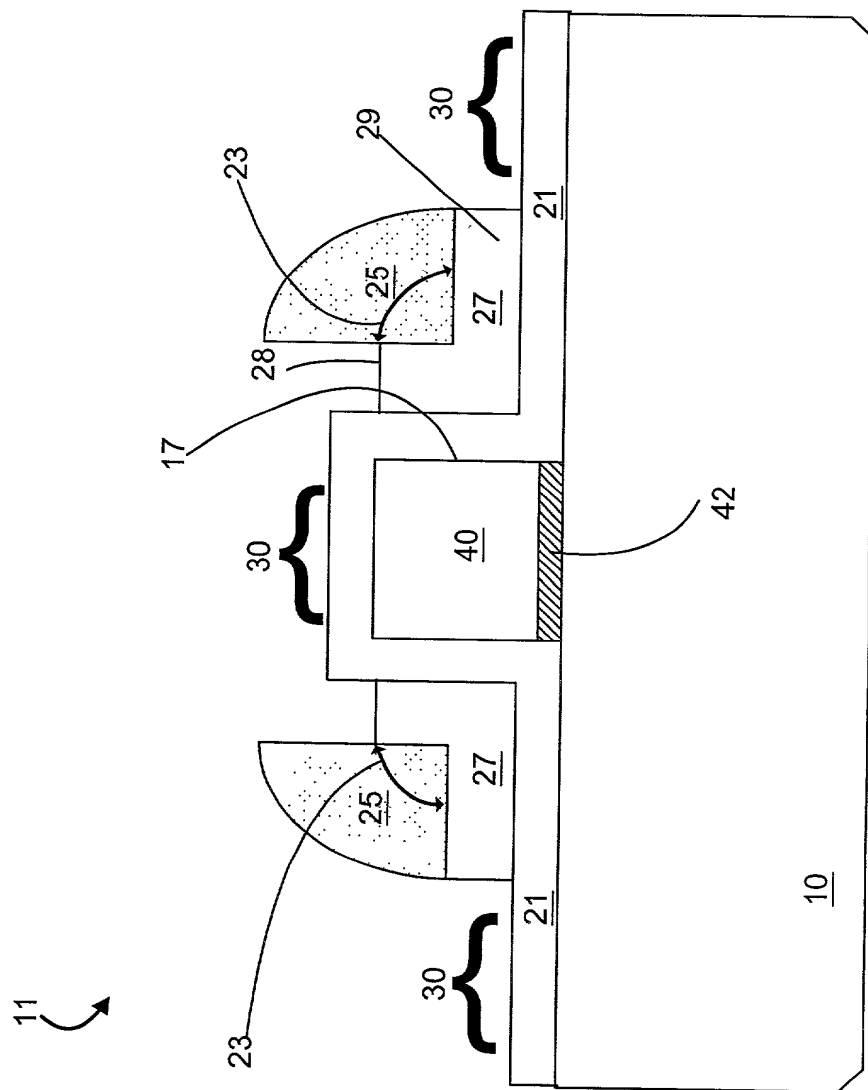


FIG. 6

FIG. 7 is a cross-sectional view of the device 10, showing the internal structure of the device 10, including the substrate 10, the gate stack 20, the gate 25, the gate 27, the gate 40, and the gate 42.

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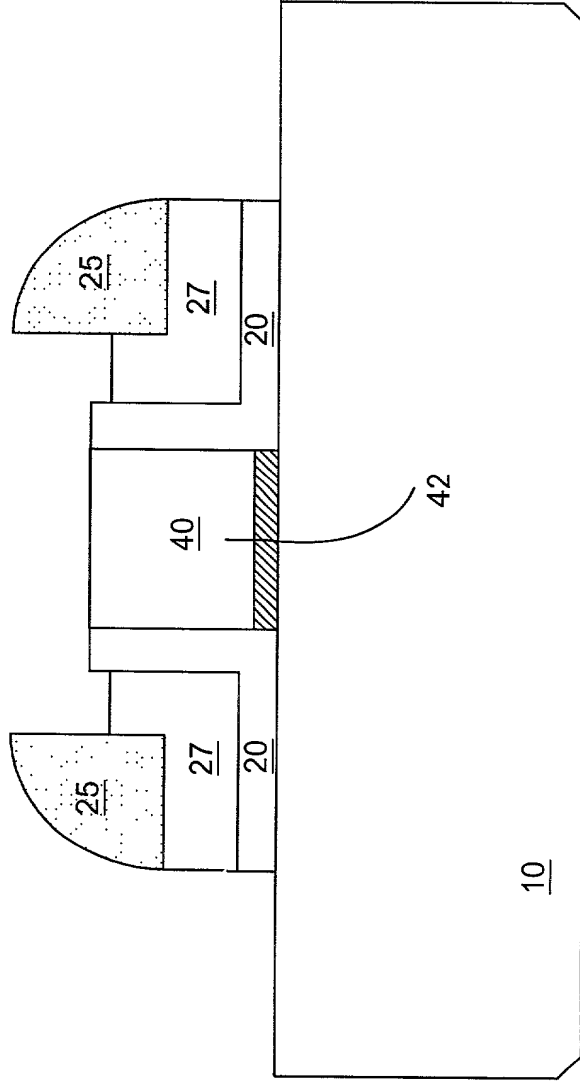


FIG. 7

11

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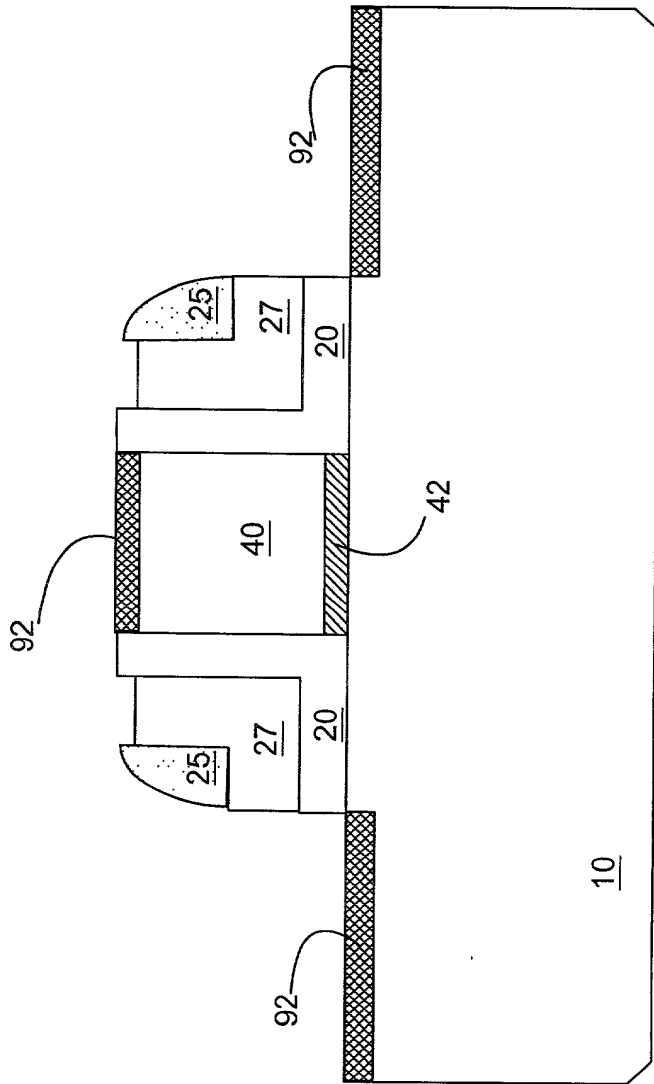


FIG. 8



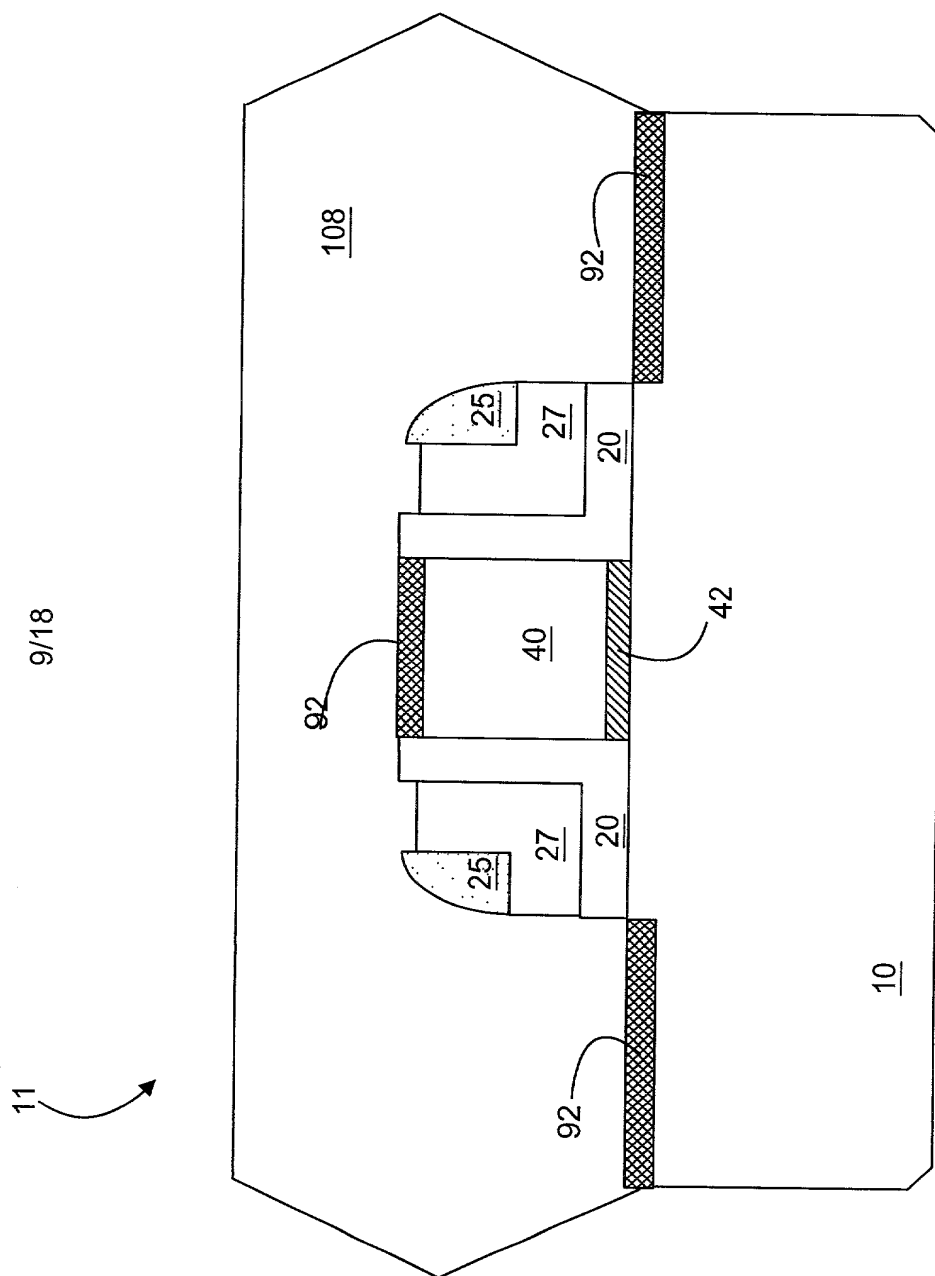


FIG. 9

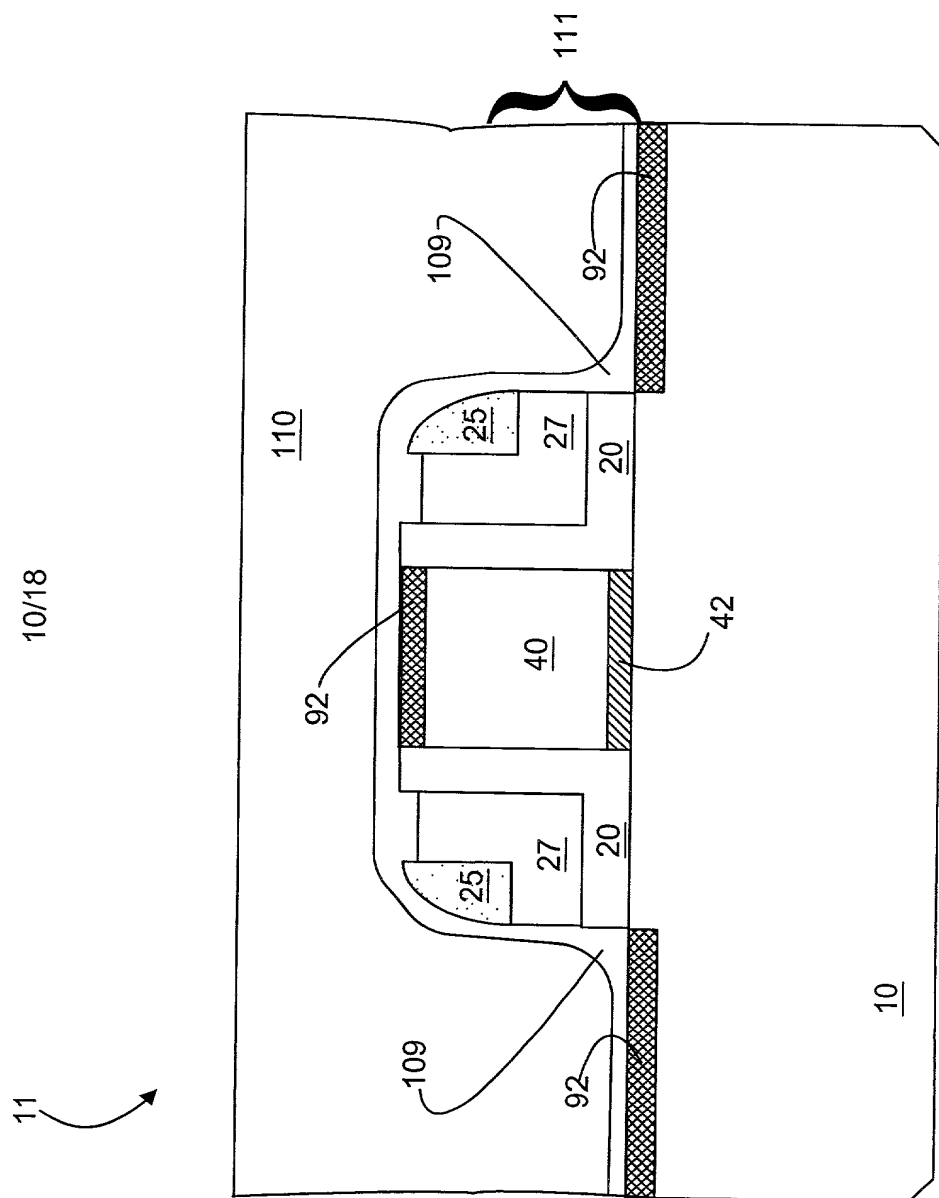


FIG. 10

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11

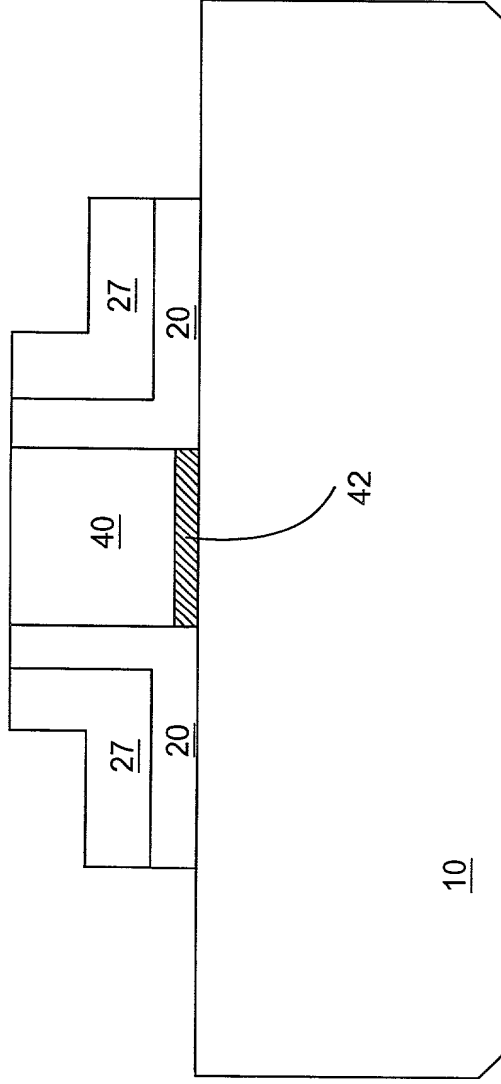


FIG. 11

11

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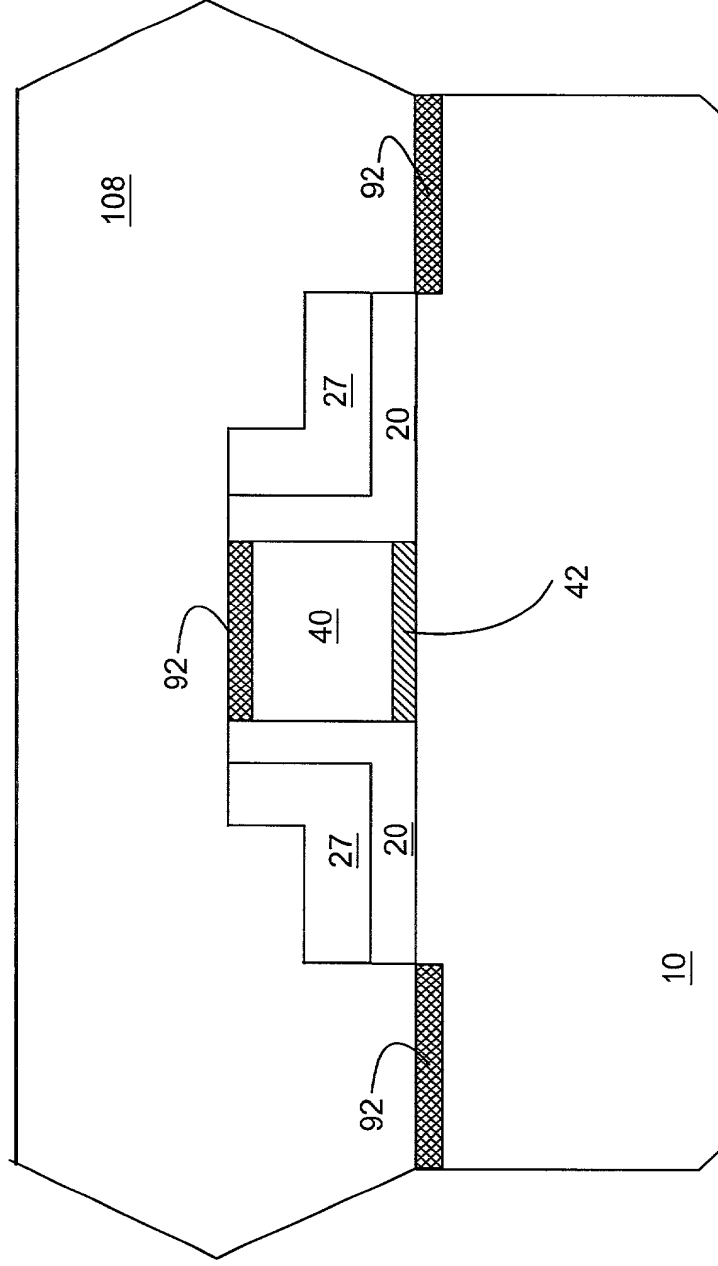


FIG. 12

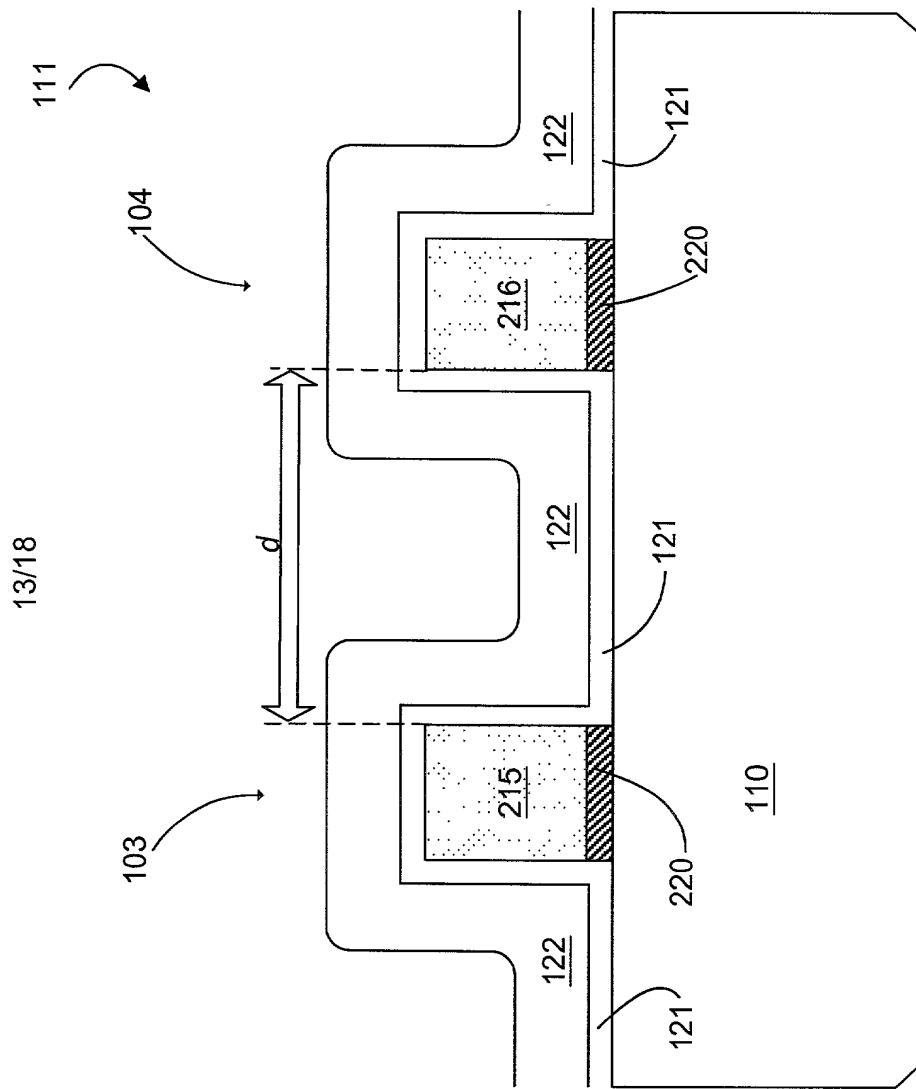


FIG. 13

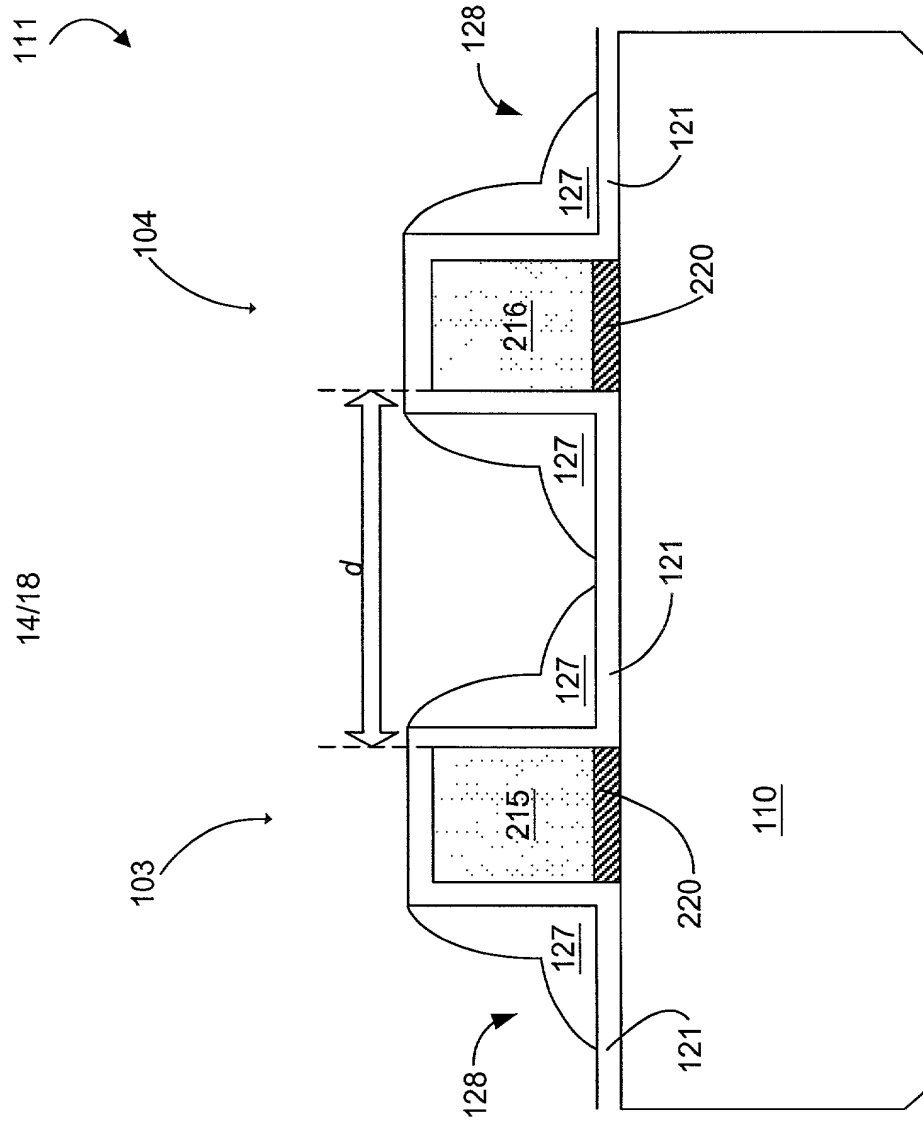


FIG. 14

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1100

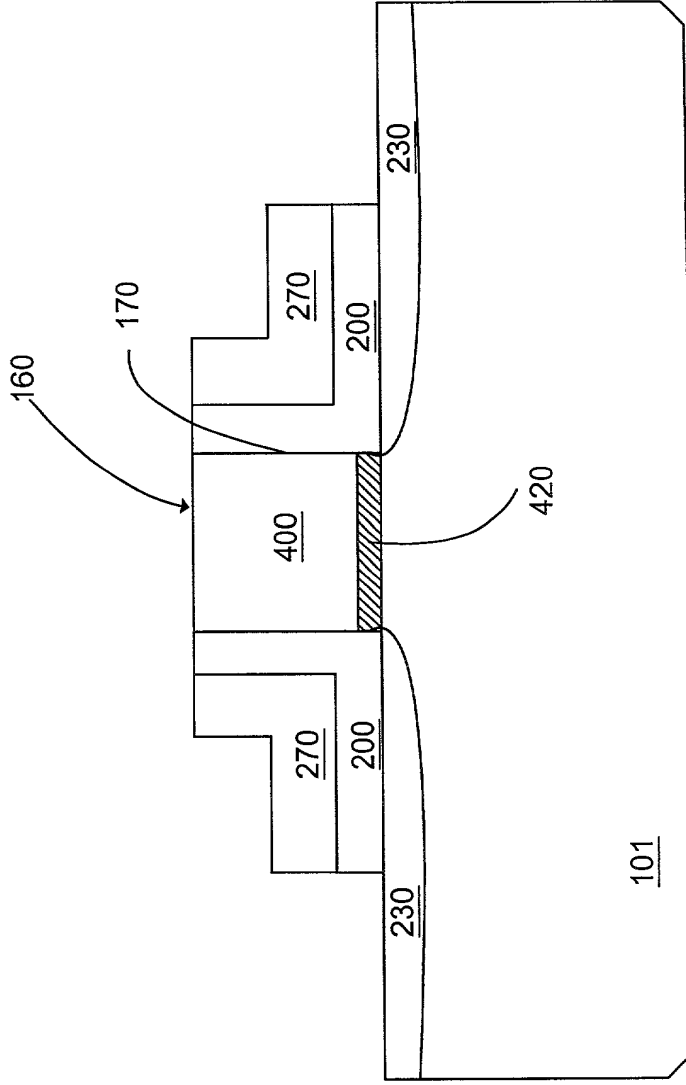


FIG. 15

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1100

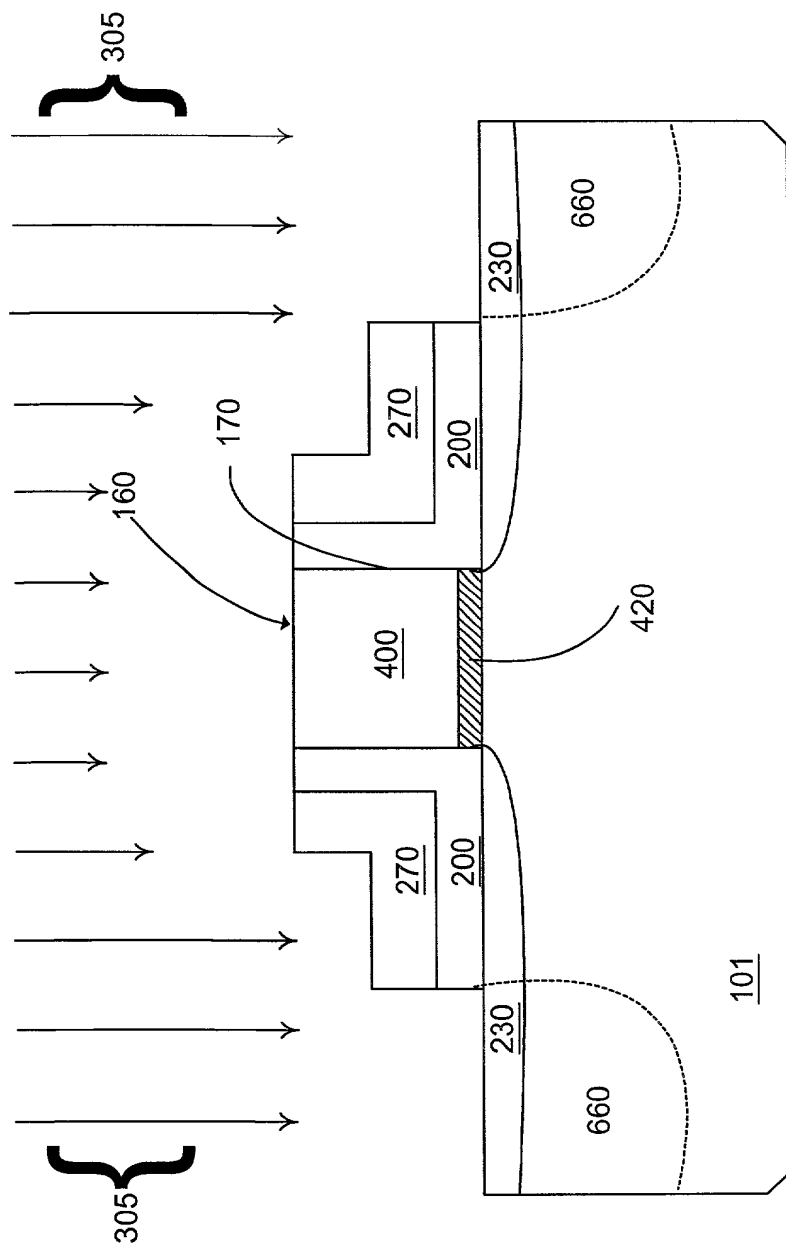



FIG. 16



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1100 

305

305

160

170

1

00

230

560

760

092

101

FIG. 17

1100

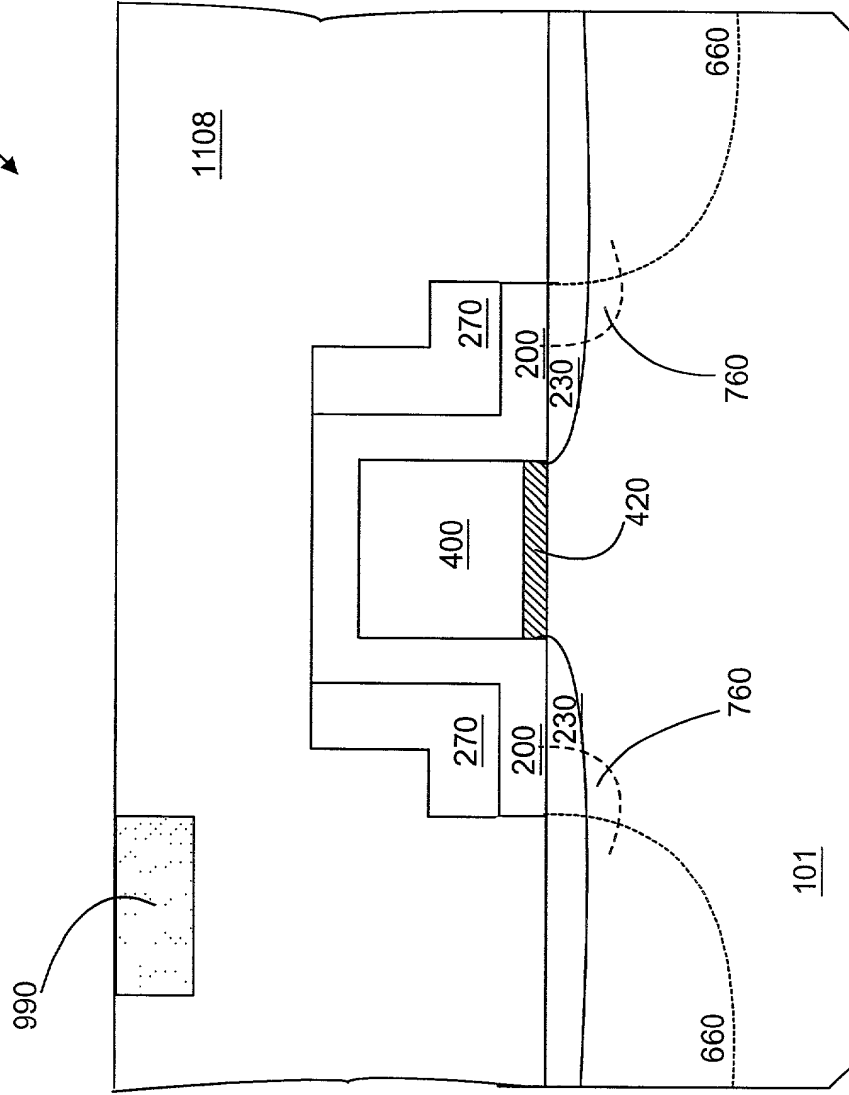


FIG. 18